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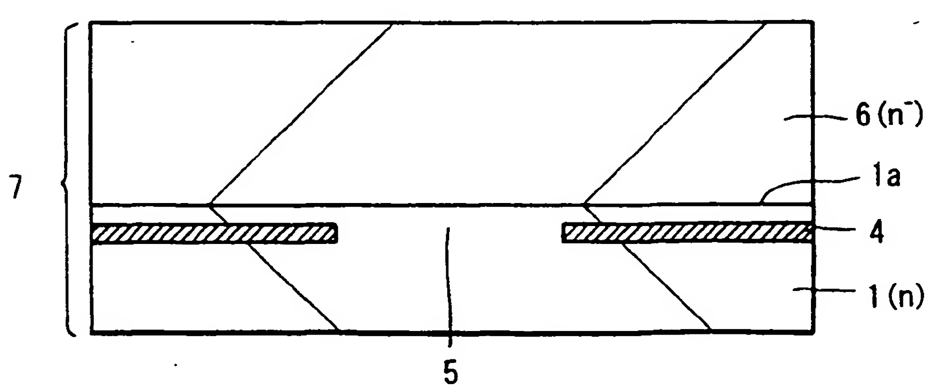
(54) Epitaxial semiconductor substrate and manufacturing method thereof; manufacturing method of semiconductor device and of solid-state imaging device

(57) Quality of epitaxial semiconductor substrates (7) treated by carbon gettering is evaluated precisely and quickly to use only good-quality ones for manufacturing good-property semiconductor devices, such as solid- state imaging devices. After carbon implanted regions (4) and carbon non-implanted regions (5) are made along the surface of a Si substrate (1) by selectively ion-implanting carbon, a Si epitaxial layer (6) is grown on the surface (1a) of the Si substrate (1) to obtain a Si epitaxial substrate (7). Recombination lifetime or surface photo voltage is measured at a portion of the Si epitaxial layer (6) located above the carbon non-implanted region (5), and the result is used to evaluate acceptability of the Si epitaxial substrate (7). Thus, strictly selected good-quality Si epitaxial substrates (7) alone are used to manufacture solid-state imaging devices or other semiconductor devices.

Fig. 5



Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to an epitaxial semiconductor substrate, manufacturing method thereof, manufacturing method of a semiconductor device and manufacturing method of a solid-state imaging device.

Description of the Related Art

[0002] As semiconductor substrates for manufacturing semiconductor devices, CZ substrates grown by CZ (Czochralski) method, MCZ substrates grown by MCZ (magnetic field Czochralski) method, and epitaxial substrates having epitaxial layers made on those substrates are often used generally.

[0003] As semiconductor substrates for solid-state imaging devices, epitaxial substrates and MCZ substrates are mainly used to reduce uneven image contrast caused by uneven dopant concentration, i.e., striation. Among them, epitaxial substrates can be made to include a low-resistance region (buried region or low-resistance substrate) under epitaxial layers for forming a device, they are effective for progressing low-voltage driving and low power consumption of solid-state imaging devices. Therefore, their wider use is still expected.

[0004] For manufacturing silicon (Si) epitaxial substrates, chemical vapor deposition (CVD) is currently used as a practical method, and four kinds of source gases are mainly used therefor. That is, hydrogen reduction process uses $SiCl_4$ or $SiHCl_3$, and reaction occurring there is expressed as follows.

$$SiCl_4 \ldots SiCl_4 + _{2H2} \rightarrow Si + 4HCl$$

$$SiHCl_3 \ldots SiHCl_3 + H_2 \rightarrow Si + 3HCl$$

Thermal decomposition method uses SiH_2Cl_2 or SiH_4, and reaction occurring there is expressed as follows.

$$SiH_2Cl_2 \ldots SiH_2Cl_2 \rightarrow Si + 2HCl$$

$$SiH_4 \ldots SiH_4 \rightarrow Si + 2H_2$$

[0005] Among these four kinds of source gases, $SiHCl_3$ is inexpensive, grows fast, and is suitable for growth of a thick epitaxial layer. And it is most used for manufacturing Si epitaxial substrates for solid-state imaging devices.

[0006] However, whichever one of those source gases is used, Si epitaxial substrates contain much impurity, especially metal impurity such as heavy metal impurity, which undesirably mixes in during deposition of the epitaxial layer. Therefore, so-called white defects due to a dark current of a solid-state imaging device cannot be reduced sufficiently, and this makes characteristics and the production yield bad.

[0007] Possible sources of metal impurities such as heavy metal impurities are stainless steel (SUS) members in a bell jar of an epitaxial growth apparatus and source material gas pipes, among others. It is assumed that, if a source gas contains a chlorine (Cl) gas, for example, it decomposes and produces HCl during growth, this corrodes stainless steel members to produce a chloride of a metal, the metal chloride is captured into the source gas, and the metal impurity is caught into the epitaxial layer. In some cases, HCl gas is intentionally introduced into a bell jar to lightly etch off the surface of a Si substrate prior to epitaxial growth of layers, and this is also a cause of corrosion of stainless steel members.

[0008] Therefore, when a Si epitaxial substrate is used to fabricate a solid-state imaging device, some gettering technique is necessary for removing metal impurities. As such gettering technique, there are, for example, intrinsic gettering for precipitating over-saturated oxygen in the Si substrate exclusively within the substrate and using it as the getter sink, and extrinsic gettering for making a polycrystalline Si film or a region doped with high-concentrated phosphorus (P) on the bottom surface of the Si substrate and utilizing a distortion stress caused thereby to make a getter sink. None of them, however, had sufficient ability as gettering method for Si epitaxial substrate, and could sufficiently reduce white defects of solid-state imaging devices.

[0009] Taking it into account, the Inventor previously proposed a method for manufacturing a Si epitaxial substrate by implanting carbon into one of surfaces of an Si substrate by a dose amount of $5 \times 10^{13} cm^{-2}$ or higher and thereafter stacking an Si epitaxial layer thereon (Japanese Patent Laid-Open Publication No. hei 6-338507). According to the method, since a getter sink assumed to be a compound of carbon and oxygen in the substrate can powerfully getter metal impurities, etc. mixing into the epitaxial layer, white defects of solid-state imaging devices could be reduced to 1/5 as compared with Si epitaxial substrates made by using conventional gettering method.

[0010] To control impurities (especially metal impurities) mixing into epitaxial layers under growth, conventionally used were (1) a method for observing pits or crystal defects in epitaxial layers after growth, (2) a method for quantitatively measuring heavy metal impurities on the surface of an epitaxial layer or in a substrate bulk by atomic absorption spectrometry, inductively coupled plasma mass spectrometry (ICP-MS), neutron activation analysis, (3) a method for conducting electric measurement such as lifetime measurement on the entirety of an epitaxial substrate by microwaves, and so on.

[0011] Among these methods, control of impurities by

microwave lifetime measurement needs no pre-treatment, and gets a result quickly and easily. Therefore, it is used widely. With regard to it, the Applicant also proposed a method for reducing white defects of solid- state imaging devices by using a Si epitaxial substrate having a lifetime whose ratio relative to the lifetime of the Si substrate before deposition of the epitaxial layer is larger than a predetermined value (Japanese Patent Laid-Open Publication No. hei 9-139408).

[0012] However, in the Si epitaxial substrate treated by carbon gettering, since the getter sink behaves as a center of electron-hole recombination, there is the problem that the measured lifetime does not reflect the amount of impurities mixing into the epitaxial layer under growth. To date, therefore, instead of measuring the life time of a Si epitaxial substrate treated by carbon gettering, the lifetime was measured from a monitor substrate prepared by forming the epitaxial layer on a Si substrate of the same batch but not treated by carbon gettering, and the result was used to evaluate the quality of the Si epitaxial substrate.

[0013] However, even among Si epitaxial substrate made in the same batch, a difference among the substrates is inevitable. Therefore, although there was a correlation to an extent between the lifetime measured from the monitor substrate and white defects of solid-state imaging devices manufactured by using Si epitaxial substrates treated by carbon gettering, the correlation was not satisfactory. It was therefore actually difficult to evaluate white defects of solid-state imaging devices, i.e., degree of impurity contamination of Si epitaxial substrates by heavy metal impurities, for example, and accurately know their acceptabiity from the result of measurement of lifetime using a monitor substrate. Furthermore, a wafer-by- wafer type has become the main current of epitaxial devices made by processing a semiconductor substrate as large as 8 inches or more in diameter, and the degree of impurity contamination varies from a sheet of the semiconductor substrate to another. Therefore, measurement of the lifetime using a monitor substrate has become almost meaningless.

[0014] Under the background, there is a strong demand for a technique which enables direct measurement of lifetime of a Si epitaxial substrate itself treated by carbon gettering, and can determine acceptability of the Si epitaxial substrate precisely and quickly.

OBJECTS AND SUMMARY OF THE INVENTION

[0015] It is therefore an object of the invention to provide an epitaxial semiconductor substrate and its manufacturing method which enables precise and quick determination of acceptability of the epitaxial semiconductor substrate treated by carbon gettering.

[0016] Another object of the invention is to provide a method for manufacturing a semiconductor device capable of precisely and quickly determining acceptability of an epitaxial semiconductor substrate treated by carbon gettering and to manufacture a good semiconductor device with a high yield by using a good epitaxial semiconductor substrate remarkably reduced in impurity contamination by heavy metal impurities, for example.

[0017] Another object of the invention is to provide a method for manufacturing a solid-state imaging device capable of precisely and quickly determining acceptability of an epitaxial semiconductor substrate treated by carbon gettering and to manufacture a good semiconductor device with a high yield by using a good epitaxial semiconductor substrate remarkably reduced in white defects.

[0018] According to the first aspect of the invention, there is provided an epitaxial semiconductor substrate having formed an epitaxial layer in which carbon is ion-implanted along a major surface of a semiconductor substrate, and an epitaxial layer made of a semiconductor is stacked on the major surface of the semiconductor substrate, comprising:

a carbon non-implanted region provided at least in one portion along the major surface of the semiconductor substrate.

[0019] According to the second aspect of the invention, there is provided a method for manufacturing an epitaxial semiconductor substrate configured to first ion-implant carbon along a major surface of a semiconductor substrate and thereafter stack an epitaxial layer made of a semiconductor on the major surface of the semiconductor substrate, characterized in:

ion implanting carbon along the major surface of the semiconductor substrate while making a carbon non-implanted region at least in one location.

[0020] According to the third aspect of the invention, there is provided a method for manufacturing a semiconductor device configured to manufacture the semiconductor device by using an epitaxial semiconductor substrate made by first ion-implanting carbon along a major surface of a semiconductor substrate and thereafter stacking an epitaxial layer made of a semiconductor on the major surface of the semiconductor substrate, characterized in:

ion-implanting carbon along the major surface of the semiconductor substrate while making a carbon non-implanted region at least in one location, then making the epitaxial layer on the major surface of the semiconductor substrate, thereafter measuring recombination lifetime or surface photo voltage of a part of the epitaxial layer located above the carbon non-implanted region, using the result thereof to evaluate acceptability of the epitaxial semiconductor substrate, and manufacturing the semiconductor device by using the epitaxial semiconductor substrate evaluated to be good.

[0021] According to the fourth aspect of the invention, there is provided a method for manufacturing a solid-state imaging device configured to manufacture the solid-state imaging device by using an epitaxial semiconductor substrate made by first ion-implanting carbon along a major surface of a semiconductor substrate and

thereafter stacking an epitaxial layer made of a semiconductor on the major surface of the semiconductor substrate, characterized in:

ion-implanting carbon along the major surface of the semiconductor substrate while making a carbon non-implanted region at least in one location, then making the epitaxial layer on the major surface of the semiconductor substrate, thereafter measuring recombination lifetime or surface photo voltage of a part of the epitaxial layer located above the carbon non-implanted region, using the result thereof to evaluate acceptability of the epitaxial semiconductor substrate, and manufacturing the solid-state imaging device by using the epitaxial semiconductor substrate evaluated to be good.

[0022] In the present invention, from the viewpoint of obtaining sufficient gettering effect by carbon, the dose amount upon ion implantation of carbon into a major surface of the semiconductor substrate is usually not less than $5x10^{13}cm^{-2}$, and preferably not less than $5x10^{13}cm^{-2}$ and not more than $5x10^{15}cm^{-2}$. Basically, configuration and size of a region of the semiconductor substrate in which carbon is not yet implanted (carbon non-implanted region) can be determined freely as far as it is possible to measure recombination lifetime or surface photo voltage (SPV) in the carbon non-implanted region and the overlying part of the epitaxial layer. However, minimum width of the carbon non-implanted region must be larger at least than the recombination lifetime or mean free path in measurement of the surface photo voltage. Normally, it is not less than the thickness of the semiconductor substrate. The carbon non-implanted region may be as large as one chip for manufacturing a semiconductor device by using the epitaxial semiconductor substrate, for example.

[0023] Measurement of the recombination lifetime or the surface photo voltage is most excellent as a method for evaluating heavy metal impurities, for example, mixing in during growth of the epitaxial layer. Measurement of the surface photo voltage is attained by making a charge of the same sign with the majority carrier to adhere onto the surface to be measured, then intermittently irradiating thereon monochromatic light of an energy larger than the band gap energy of the substrate, and measuring changes in barrier height of the surface ($-q\Delta V$) due to the minority carrier generated thereby and moving toward and accumulating on the surface depletion layer. $-q\Delta V$ is the SPV value. As the SPV method, there are a method of adjusting the amount of the irradiated light to make the SPV value constant (constant SPV method) and a method of measuring the SPV value while making the amount of irradiated light constant in the region exhibiting a linear relation between the SPV value and the amount of irradiated light (linear SPV method). The SPV method, in general, uses the diffusion length (L) of the minority carrier as the scale of cleanness of the substrate. The longer the diffusion length, the cleaner the substrate.

[0024] In the present invention, determination of acceptability of the epitaxial semiconductor substrate is attained, when using recombination lifetime measurement, typically by measuring recombination lifetime of the semiconductor substrate in the carbon non-implanted region (τ_{sub}), also measuring the recombination lifetime of the epitaxial layer in the portion above the carbon non-implanted region (τ_{epi}), and evaluating whether or not the ratio of the measured value of the recombination lifetime of the epitaxial layer above the carbon non-implanted region relative to the measured value of the recombination life time of the semiconductor substrate in the carbon non-implanted region (τ_{epi}/τ_{sub}) is larger than a predetermined value, preferably not smaller than 1/3, and more preferably not smaller than 2/3. For measuring the surface photo voltage, especially using linear SPV method, determination of acceptability of the epitaxial semiconductor substrate is attained by measuring diffusion length of the semiconductor substrate in the carbon non-implanted region (L_{sub}), also measuring the diffusion length of the epitaxial layer in the portion above the carbon pre-implanted region (L_{epi}), and evaluating whether or not the ratio of the measured value of the diffusion length of the epitaxial layer above the carbon non-implanted region relative to the measured value of the diffusion length of the semiconductor substrate in the carbon non-implanted region (L_{epi}/L_{sub}) is larger than a predetermined value, preferably not smaller than 1/3, and more preferably not smaller than 2/3. When using diffusion measurement by SPV method, determination of acceptability need not rely on the ratio of measured values of diffusion length (L_{epi}/L_{sub}), but may be based on whether or not L_{epi} is larger than a predetermined value, suitably not less than 200 μm, and more preferably not less than 400 μm.

[0025] In the present invention, the solid-state imaging device may be an amplifying type solid-state imaging device or a CMOS solid-state imaging device instead of the CCD solid-state imaging device. The semiconductor device may be any one of various devices such as bipolar LSI, MOSLSI (such as DRAM) or bipolar CMOSLSI instead of those solid-state imaging devices.

[0026] In the present invention having the above-summarized construction, by using a location of the epitaxial layer above the carbon non-implanted region of the semiconductor substrate as the measured region, recombination lifetime or surface photo voltage reflecting the true amount of impurities mixed in during growth of the epitaxial layer can be measured directly from the epitaxial semiconductor substrate treated by carbon gettering, and acceptability of the epitaxial semiconductor substrate can be determined precisely and quickly on the basis of the result of the measurement. Then, by using the epitaxial semiconductor substrate evaluated to be good and remarkably reduced in impurity contamination such as heavy metal impurities to manufacture a semiconductor device such as a solid-state imaging device, the invention can ensure high-yield fabrication of a solid- state imaging device or other semiconductor

device with remarkably reduced white defects and a good property.

[0027] The above, and other, objects, features and advantages of the present invention will become readily apparent from the following detailed description thereof which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

Figs. 1 to 5 are cross-sectional views for explaning a method for manufacturing a Si epitaxial substrate according to the first embodiment of the invention;

Fig. 6 is a plan view of an example of the Si epitaxial substrate manufactured by the first embodiment;

Figs. 7 to 11 are cross-sectional views for explaning a method for manufacturing a CCD solid-state imaging device according to the second embodiment of the invention; and

Fig. 12 is a graph showing correlation between recombination lifetime measured on a Si epitaxial substrate in a location above a carbon non- implanted region and white defects of a CCD solid-state imaging device manufactured by using the Si epitaxial substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] Embodiments of the invention are explained below with reference to the drawings. In all of the drawings illustrating the embodiments, the same or equivalent elements or components are denoted by common reference numerals.

[0030] Figs. 1 through 5 show a manufacturing method of a Si epitaxial substrate according to the first embodiment of the invention.

[0031] In the first embodiment, first prepared is a (100)-oriented n-type CZ-Si substrate 1, for example, which is cut out from a single-crystalline Si ingot grown by CZ method and fabricated by mirror polishing, as shown in Fig. 1. Reference numeral 1a denotes a mirror surface. The CZ-Si substrate 1 is doped with P as an n-type impurity, and its resistivity is 8 to 12 Ωcm, for example, 10 Ωcm. Diameter of the CZ-Si substrate 1 is , for example, 5 inches.

[0032] After the CZ-Si substrate 1 is cleaned by RCA method, as shown in Fig. 2, it is thermally oxidized at 1000°C, for example, by dry oxidation, for example to form an oxide film 2 made of SiO_2 on the mirror surface 1a. Thickness of the oxide film 2 is, for example, 20 nm.

[0033] Next, as shown in Fig. 3, a resist pattern 3 opening at a portion corresponding to a region for implanting carbon ions is made on the oxide film 2 by lithography. After that, using the resist pattern 3 as a mask, carbon is ion-implanted into the CZ-Si substrate 1. For carbon ion implantation, acceleration energy of 150 keV and dope amount of $1x10^{15}cm^{-2}$ are used, for example. In this case, projected range (R_p) of carbon is approximately 0.32 µm, and peak concentration of carbon is approximately $1x10^{19}cm^{-3}$.

[0034] Then, the resist pattern 3 is removed, and the CZ-Si substrate 1 is cleaned by RCA method. After that, the CZ-Si substrate 1 is annealed in a nitrogen atmosphere, for example, at 1000°C, for example, for 10 minutes. As a result of annealing, a carbon implanted region 4 having its peak concentration at a position deeper than the mirror surface 1a of the CZ-Si substrate 1 and a carbon non-implanted region 5 are made as shown in Fig. 4. The reason why the carbon peak-concentrated position in the carbon implanted region 4 is deeper than the mirror surface 1a lies in the requirement for preventing deterioration of crystalline quality of an n^-- type Si epitaxial layer 6 grown in the next step. Although the annealing is conducted in the nitrogen atmosphere after carbon ion implantation for the purpose of recovering the crystalline property of the CZ-Si substrate 1 near the mirror surface 1a, which is once changed to an amorphous phase by ion implantation, it may be omitted under certain implantation conditions.

[0035] After that, the oxide film 2 is removed by etching using an etchant which contains HF solution, for example. thereafter, as shown in Fig. 5C, the n^--type Si epitaxial layer 6 is grown at a temperature around 1120°C, for example, by CVD using $SiHCl_3$, for example, as the source gas to complete the Si epitaxial substrate 7. The n^--type Si epitaxial layer 6 is doped with P, for example, as its n-type impurity. Its resistivity is 40 to 50 Ωcm, for example, and the thickness is 8 µm, for example.

[0036] An example of the Si epitaxial substrate 7 manufactured in this manner is shown in Fig. 6. As shown here, this example has formed square carbon non-implanted regions 5 at two locations of the CZ-Si substrate 1 at the center of the Si epitaxial substrate 7 and near an orientation flat 7a, respectively. Sides of these carbon non-implanted regions 5 are parallel to directions parallel and normal to the orientation flat 7a, for example. size of each carbon non-implanted region 5 is, for example, 10 mm x 10 mm or 8 mm x 8 mm.

[0037] To estimate acceptability of the Si epitaxial substrate 7 made in the above-explained process, recombination lifetime is measured by microwaves in the n^--type Si epitaxial layer 6 above the carbon non- implanted region 5, and only Si epitaxial substrates 7 demonstrating a good result are selected. A result of measurement on recombination lifetime is evaluated in the following manner. That is, respectively measured are recombination lifetime τ_{sub} of the carbon non-implanted region 5 of the CZ-Si substrate 1 before growth of the n^--type Si epitaxial layer 6 and lifetime τ_{epi} of a part of the Si epitaxial substrate 7 above the carbon non- implanted region 5. When τ_{epi}/τ_{sub} is 2/3 or more, for example, the Si epitaxial substrate 7 is classified to be

good.

[0038] Figs. 7 through 11 illustrate a manufacturing method of a CCD solid-state imaging device according to the second embodiment of the invention.

[0039] In the second embodiment, first prepared is a good Si epitaxial substrate 7 remarkably reduced in impurity contamination such as heavy metal impurities, which has been selected in the above-explained manner.

[0040] Next, as shown in fig. 7, a p-type well region 8 is formed in the n^--type Si epitaxial layer 6 of the Si epitaxial substrate 7 by ion implantation, for example. After that, an insulating film 9 of SiO_2, for example, is made on the surface of the p-type well region 8 by thermal oxidation, for example. Then, by selectively ion-implanting an n-type impurity and a p-type impurity into the p-type well region 8, respectively, to form an n-type transfer channel region 10 forming a vertical transfer register, p^+-type channel stop region 11 adjacent thereto and a p^+-type well region 12 under the n-type transfer channel region 10.

[0041] Thereafter, as shown in Fig. 8, formed on the insulating film 9 is a transfer electrode 15 via an insulating film 13 such as Si_3N_4 film and an insulating film 14 such as SiO_2 film, for example. The insulating films 9, 13 and 14 form a gate insulating film. When the insulating films 9 and 14 are SiO_2 films, and the insulating film 13 is a Si_3N_4 film, the gate insulating film is a so-called ONO film. The transfer electrode 15 is made of a polycrystalline Si film doped with an impurity such as P.

[0042] Next as shown in Fig. 9, n^+-type regions 16 are made by selectively ion-implanting an n-type impurity into locations of the p-type well region 8 to be made as photo sensor portions. The pn junction made of the n^+-type region 16 and the p-type well region 8 forms a photo diode to serve as a photo sensor (photoelectric converter).

[0043] Next as shown in Fig. 10, a p^{++}-type region 17 is made by ion-implanting a p-type impurity into he surface of the n^+-type region 16.

[0044] After that, as shown in Fig. 11, an inter-layer insulating film 18 of SiO_2, for example, is made on the entire substrate surface, and an Al shade film 19 is formed on the part of the inter-layer insulating film 18 above the transfer electrode 15.

[0045] The intended CCD solid-state imaging device is thus completed.

[0046] Fig. 12 shows a result of measurement on relationship between recombination lifetime measured at a central portion of the Si epitaxial substrate 7 and white defects of the CCD solid-state imaging device manufactured by using the Si epitaxial substrate 7. As shown in Fig. 12, there is apparent correlation between recombination lifetime and white defects, and white defects increase as the recombination lifetime decreases.

[0047] Also regarding white defects of the CCD solid-state imaging device made in a portion overlapping the carbon non-implanted region 5 in the Si epitaxial substrate 7, the result of measurement was substantially similar to the result of measurement of white defects of the CCD solid-state imaging device formed in a portion of the carbon implanted region 4 in the Si epitaxial substrate 7. This is probably because the diffusion length of metal impurities affecting white defects is sufficiently larger than the size of the carbon non- implanted region 5 at the temperature for heat treatment in the process for manufacturing the device.

[0048] As explained above, according to the second embodiment, since the CCD solid-state imaging device is manufactured by using a previously selected good-quality Si epitaxial substrate 7 in which impurity contamination by heavy metal impurities, or the like, is remarkably reduced, a CCD solid-state imaging device remarkably reduced in white defects and excellent in property can be manufactured with a high yield. Additionally, although conventional techniques could locate only after making solid-state imaging devices, the second embodiment, configured to select only good products with a high accuracy still in the state of Si epitaxial substrates 7, can remove futility by fabrication of defective CCD solid-state-imaging devices using defective Si epitaxial substrates 7 with much impurity contamination by heavy metal impurities, for example, and hence remarkably reduce the manufacturing cost of CCD solid-state imaging devices.

[0049] Having described specific preferred embodiments of the present invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one skilled in the art without departing from the scope of the invention as defined in the appended claims.

[0050] For example, structures, configurations, processes and numerical values introduced in the first and second embodiments are only examples, and any appropriate other structures, configurations, processes and numerical values may be employed, if necessary.

[0051] Specifically as to the first embodiment, although two carbon pe-implanted regions 5 are formed in the Si epitaxial substrate 7, the number of the carbon non-implanted region 5 may be only one, or three or more. For example, as shown by the dot-and-dash lines in Fig. 6, additional three carbon non-implanted regions 5 may be made to form five carbon non-implanted regions in total.

[0052] Regarding the second embodiment, explained as making the n^+-type region 16 in the p-type well region 8 formed in the n^--type Si epitaxial layer 6 on the n-type Si epitaxial substrate 7 such that the n^+-type region 16 and the p-type well region 8 form a photo diode as the photo sensor, it may be modified to form a photo diode by making an n-type region in the p-type Si epitaxial layer.

[0053] Moreover, needless to say, the invention is applicable also to fabrication of CCD solid-state imaging

devices of a type having an in-layer lens.

[0054] Furthermore, although the first embodiment has been explained as evaluating acceptability of the Si epitaxial substrate 7, the result of the evaluation may be used also for contamination control of the epitaxial growth apparatus used therefor. In this manner, contamination control of the epitaxial growth apparatus can be made without using a monitor substrate.

[0055] As described above, according to the epitaxial semiconductor substrate by the present invention having formed at least one carbon non-implanted region along one major surface of the semiconductor substrate, acceptability of the epitaxial semiconductor substrate treated by carbon gettering can be evaluated precisely and quickly by measuring recombination lifetime or surface photo voltage of the epitaxial layer in the location above the carbon non-implanted region.

[0056] According to the manufacturing method of an epitaxial semiconductor substrate by the invention, configured to ion-implant carbon onto one major surface of the semiconductor substrate and make at least one carbon non-implanted region, acceptability of the epitaxial semiconductor substrate treated by carbon gettering can be evaluated precisely and quickly by measuring recombination lifetime or surface photo voltage of the epitaxial layer in the location above the carbon non-implanted region.

[0057] According to the manufacturing method of a semiconductor device by the present invention, which is configured to manufacture a semiconductor device by using a good-quality epitaxial semiconductor substrate with remarkably reduced impurity contamination by heavy metal impurities, for example, semiconductor devices excellent in property can be manufactured with a high yield.

[0058] According to the manufacturing method of a solid-state imaging device by the present invention, which is configured to manufacture a solid-state imaging device by using a good-quality epitaxial semiconductor substrate with remarkably reduced impurity contamination by heavy metal impurities, for example, solid-state imaging devices remarkably reduced in white defects and excellent in property can be manufactured with a high yield.

Claims

1. An epitaxial semiconductor substrate having formed an epitaxial layer (6) in which carbon is ion-implanted along a major surface (1a) of a semiconductor substrate (1), and an epitaxial layer (6) made of a semiconductor is stacked on said major surface (1a) of the semiconductor substrate (1), comprising:

   a carbon non-implanted region (5) provided at least in one portion along said major surface (1a) of said semiconductor substrate (1).

2. The epitaxial semiconductor substrate according to claim 1 wherein a part of said epitaxial layer (6) located above said carbon non-implanted region (5) is used to measure recombination lifetime or surface photo voltage thereof.

3. The epitaxial semiconductor substrate according to claim 1 wherein minimum width of said carbon non-implanted region (5) is larger than the mean free path upon measurement of said recombination lifetime or surface photo voltage.

4. The epitaxial semiconductor substrate according to claim 1 wherein minimum width of said carbon non-implanted region (5) is not less than the thickness of said semiconductor substrate (1).

5. A method for manufacturing an epitaxial semiconductor substrate (7) configured to first ion-implant carbon along a major surface (1a) of a semiconductor substrate (1) and thereafter stack an epitaxial layer (6) made of a semiconductor on said major surface (1a) of said semiconductor substrate (1), characterized in:

   ion implanting carbon along said major surface (1a) of said semiconductor substrate while making a carbon non-implanted region (5) at least in one location.

6. The method for manufacturing an epitaxial semiconductor substrate (7) according to claim 5 wherein a part of said epitaxial layer (6) located above said carbon non-implanted region (5) is used to measure recombination lifetime or surface photo voltage thereof.

7. The method for manufacturing an epitaxial semiconductor substrate (7) according to claim 5 wherein minimum width of said carbon non-implanted region(5) is larger than the mean free path upon measurement of said recombination lifetime or surface photo voltage.

8. The method for manufacturing an epitaxial semiconductor substrate (7) according to claim 5 wherein minimum width of said carbon non-implanted region (5) is not less than the thickness of said semiconductor substrate (1).

9. A method for manufacturing a semiconductor device configured to manufacture the semiconductor device by using an epitaxial semiconductor substrate (7) made by first ion-implanting carbon along a major surface (1a) of a semiconductor substrate (1) and thereafter stacking an epitaxial layer (6) made of a semiconductor on said major surface (1a) of said semiconductor substrate (1), characterized in:

ion-implanting carbon along the major surface (1a) of said semiconductor substrate (1) while making a carbon non-implanted region (5) at least in one location, then making said epitaxial layer (6) on the major surface (1a) of said semiconductor substrate (1), thereafter measuring recombination lifetime or surface photo voltage of a part of said epitaxial layer (6) located above said carbon non-implanted region (5), using the result thereof to evaluate acceptability of said epitaxial semiconductor substrate (7), and manufacturing the semiconductor device by using said epitaxial semiconductor substrate (7) evaluated to be good.

10. The method for manufacturing a semiconductor device according to claim 9 wherein minimum width of said carbon non-implanted region (5) is larger than the mean free path upon measurement of said recombination lifetime or surface photo voltage.

11. The method for manufacturing a semiconductor device according to claim 9 wherein minimum thickness of said carbon non-implanted region (5) is not less than the thickness width of said semiconductor substrate (1).

12. The method for manufacturing a semiconductor device according to claim 9 wherein acceptability of said epitaxial semiconductor substrate (7) is evaluated by measuring recombination lifetime of said carbon non- implanted region (5) of said semiconductor substrate (1), measuring recombination lifetime of a part of said epitaxial layer (6) above said carbon non-implanted region (5), and evaluating whether the ratio of the measured value of recombination lifetime of the part of said epitaxial layer (6) above said carbon non-implanted region (5) to the measured value of recombination lifetime of said carbon non-implanted region (5) of said semiconductor substrate (1) is larger than a predetermined value or not.

13. The method for manufacturing a semiconductor device according to claim 9 wherein acceptability of said epitaxial semiconductor substrate (7) is evaluated by measuring surface photo voltage of said carbon non- implanted region (5) of said semiconductor substrate (1), measuring surface photo voltage of a part of said epitaxial layer (6) above said carbon non-implanted region (5), and evaluating whether the ratio of the measured value of surface photo voltage of the part of said epitaxial layer (6) above said carbon non-implanted region (5) to the measured value of surface photo voltage of said carbon non-implanted region (5) of said semiconductor substrate (1) is larger than a predetermined value or not.

14. A method for manufacturing a solid-state imaging device configured to manufacture the solid- state imaging device by using an epitaxial semiconductor substrate (7) made by first ion-implanting carbon along a major surface (1a) of a semiconductor substrate (1) and thereafter stacking an epitaxial layer (6) made of a semiconductor on said major surface of said semiconductor substrate, characterized in:

ion-implanting carbon along the major surface (1a) of said semiconductor substrate (1) while making a carbon non-implanted region (5) at least in one location, then making said epitaxial layer (6) on the major surface (1a) of said semiconductor substrate (1), thereafter measuring recombination lifetime or surface photo voltage of a part of said epitaxial layer (6) located above said carbon non-implanted region (5), using the result thereof to evaluate acceptability of said epitaxial semiconductor substrate (7), and manufacturing the solid-state imaging device by using said epitaxial semiconductor substrate (7) evaluated to be good.

15. The method for manufacturing a solid-state imaging device according to claim 14 wherein minimum width of said carbon non-implanted region (5) is larger than the mean free path upon measurement of said recombination lifetime or surface photo voltage.

16. The method for manufacturing a solid-state imaging device according to claim 14 wherein minimum width of said carbon non-implanted region (5) is not less than the thickness of said semiconductor substrate (1).

17. The method for manufacturing a solid-state imaging device according to claim 14 wherein acceptability of said epitaxial semiconductor substrate (7) is evaluated by measuring recombination lifetime of said carbon non-implanted region (5) of said semiconductor substrate (1), measuring recombination lifetime of a part of said epitaxial layer (6) above said carbon non-implanted region (5), and evaluating whether the ratio of the measured value of recombination lifetime of the part of said epitaxial layer (6) above said carbon non-implanted region (5) to the measured value of recombination lifetime of said carbon non-implanted region (5) of said semiconductor substrate (1) is larger than a predetermined value or not.

18. The method for manufacturing a solid-state imaging device according to claim 14 wherein acceptability of said epitaxial semiconductor substrate (7) is evaluated by measuring surface photo voltage of said carbon non-implanted region (5) of said semiconductor substrate (1), measuring surface photo voltage of a part of said epitaxial layer (6) above said

carbon non-implanted region (5), and evaluating whether the ratio of the measured value of surface photo voltage of the part of said epitaxial layer (6) above said carbon non-implanted region (5) to the measured value of surface photo voltage of said carbon non-implanted region (5) of said semiconductor substrate (1) is larger than a predetermined value or not.

Fig. 1

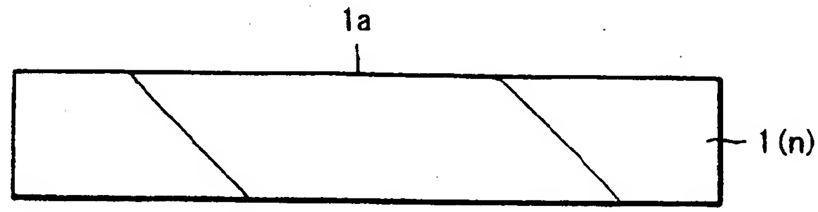


Fig. 2

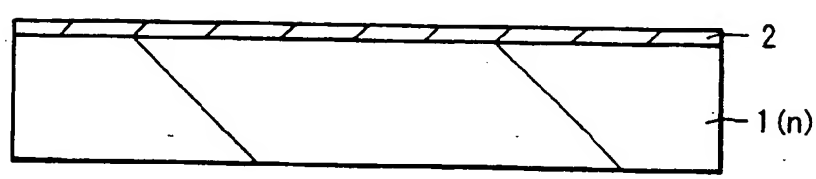


Fig. 3

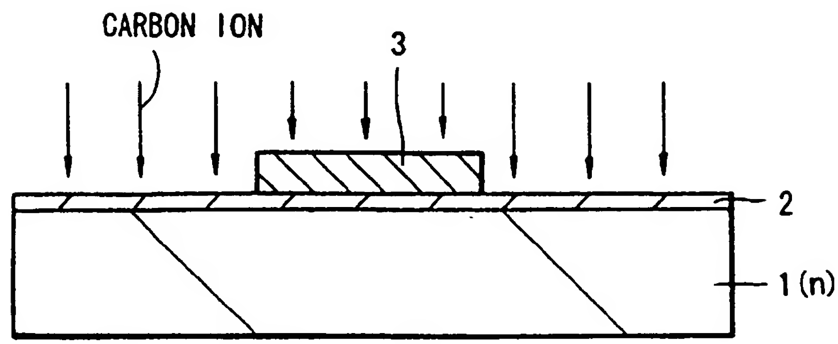


Fig. 4

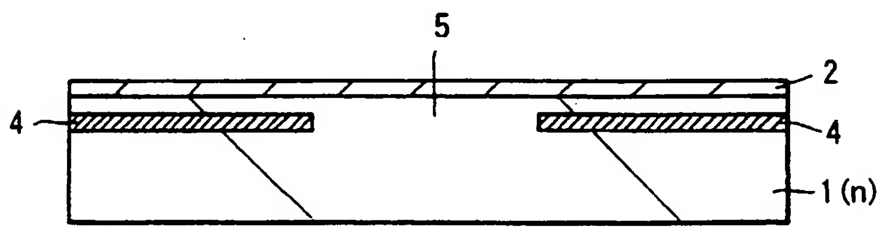


Fig. 5

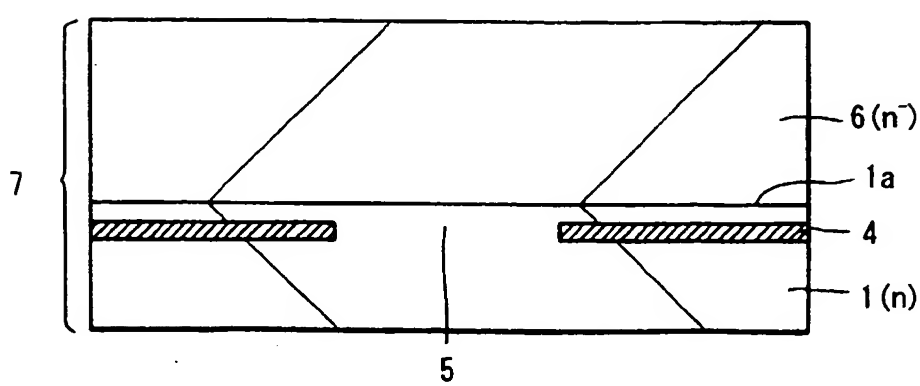


Fig. 6

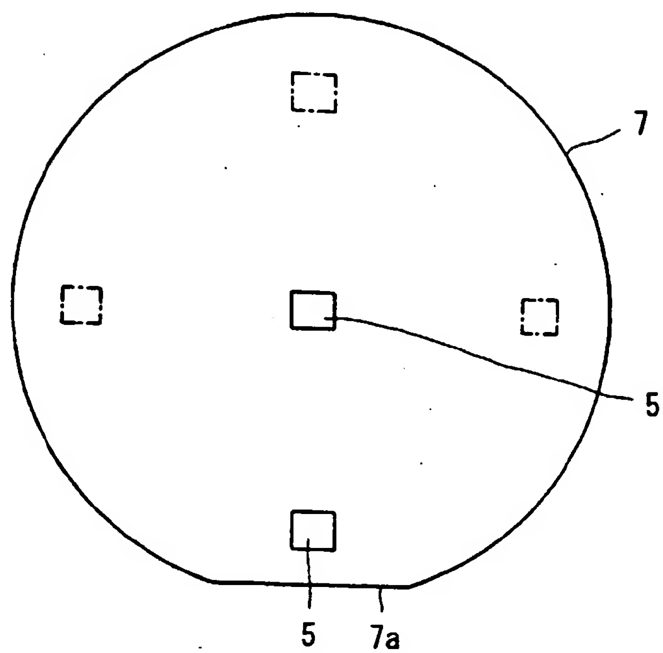


Fig. 7

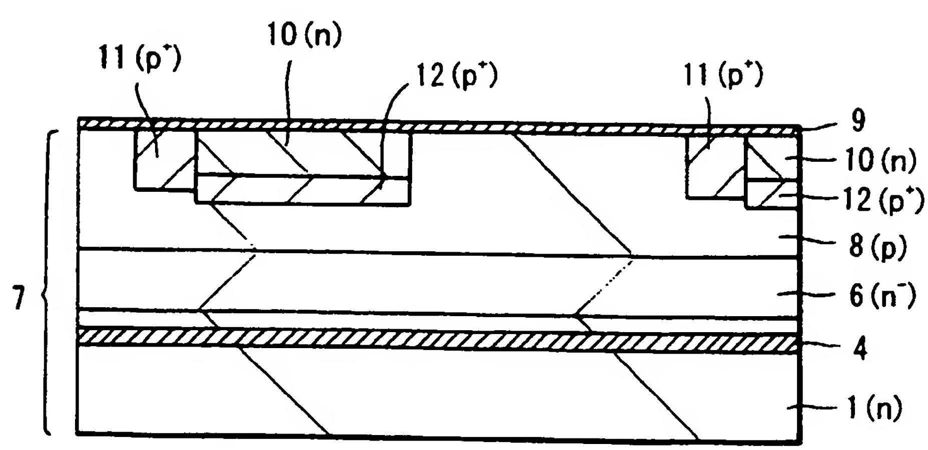


Fig. 8

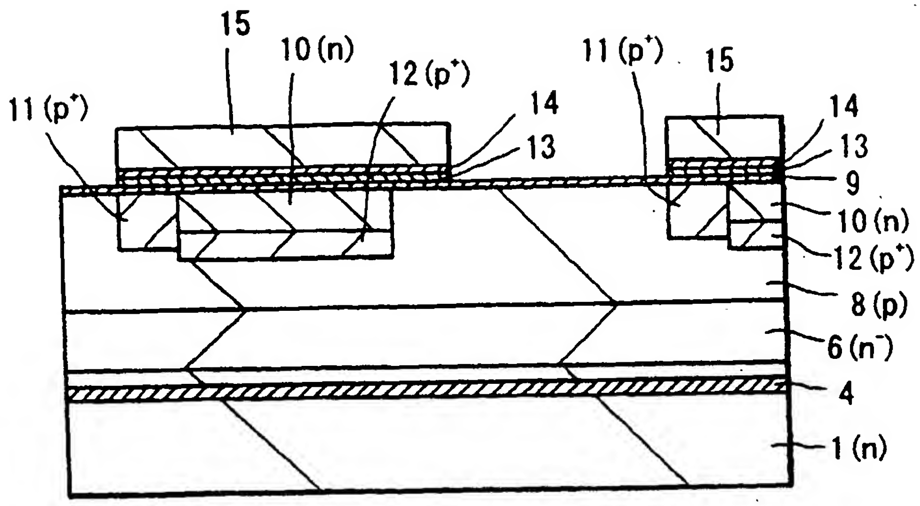

15
10 (n)
12 (p⁺)
11 (p⁺)
14
13
11 (p⁺)
15
14
13
9
10 (n)
12 (p⁺)
8 (p)
6 (n⁻)
4
1 (n)

Fig. 9

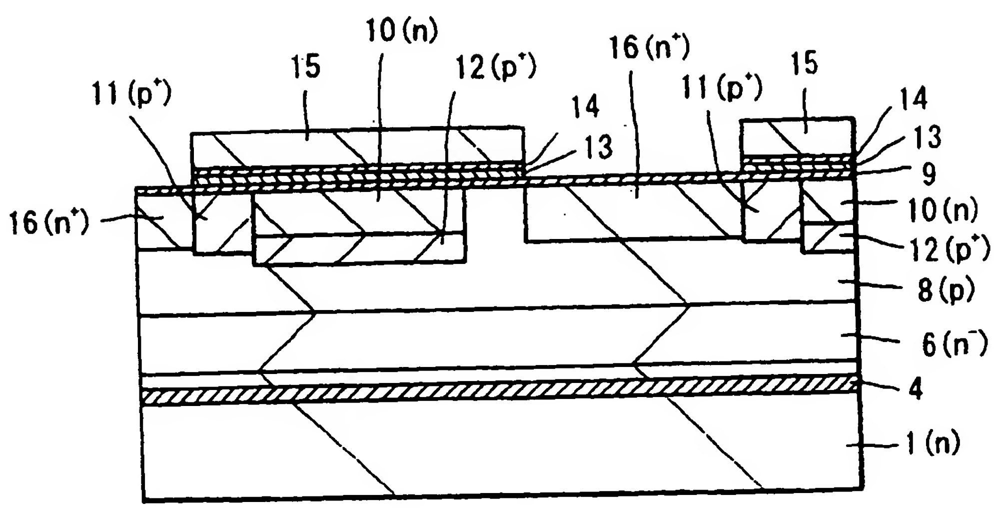
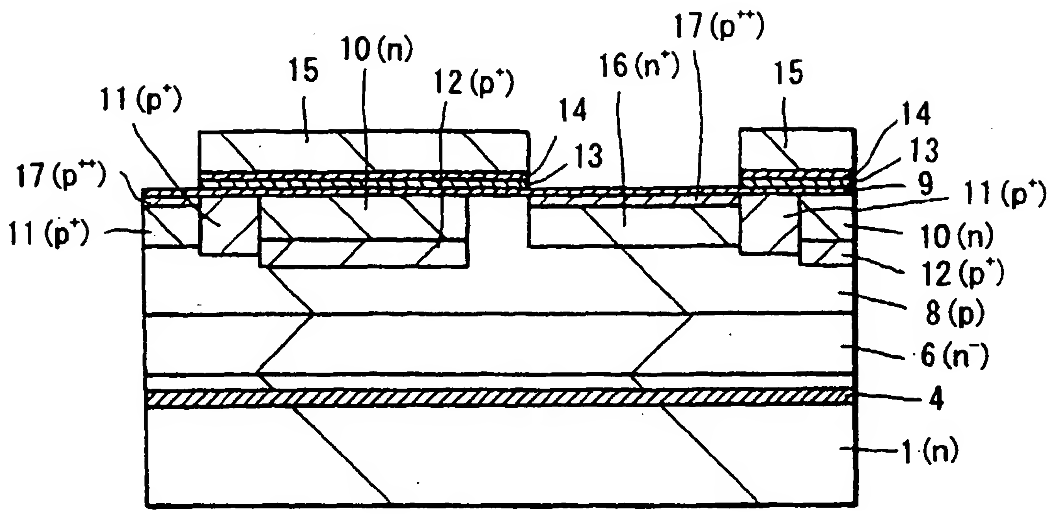
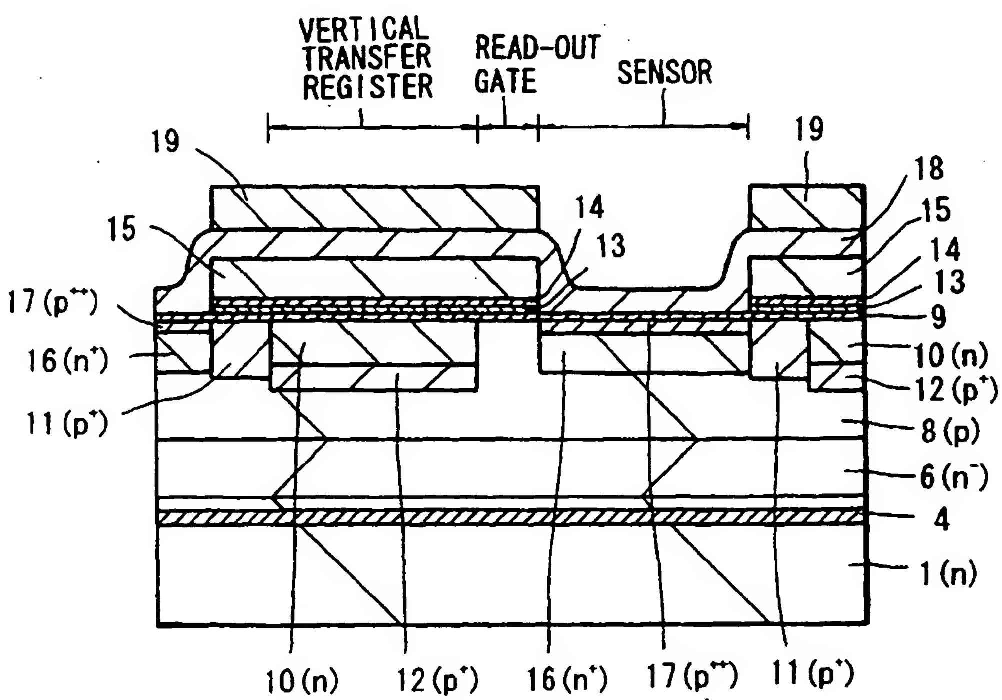

10 (n)
15
12 (p⁺)
11 (p⁺)
16 (n⁺)
16 (n⁺)
11 (p⁺)
15
14
13
14
13
9
10 (n)
12 (p⁺)
8 (p)
6 (n⁻)
4
1 (n)

Fig. 10



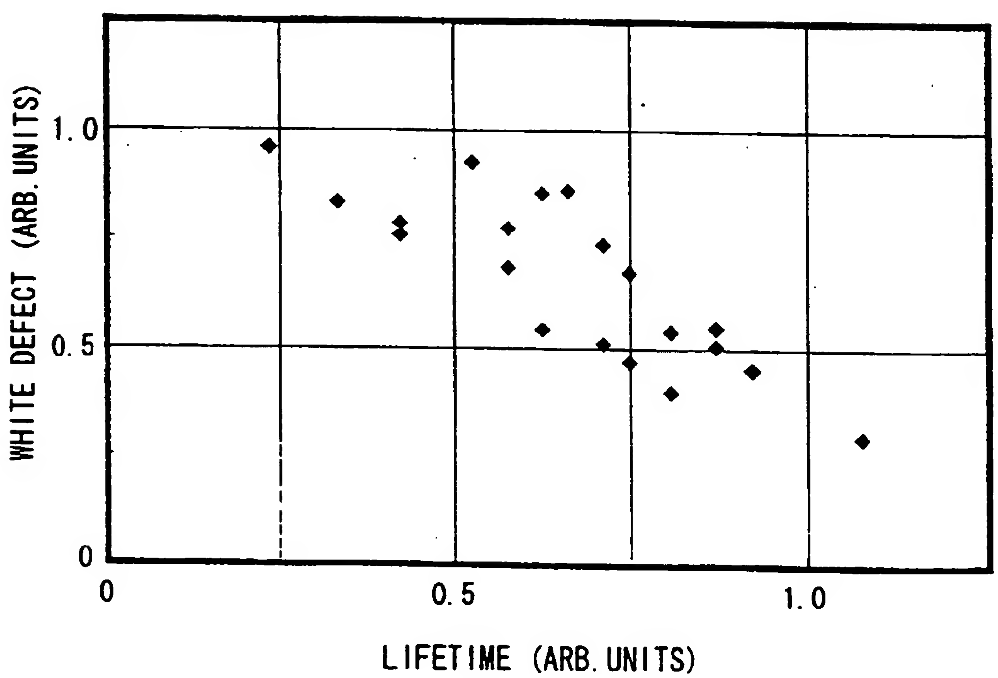
17 (p++)
10 (n)
15
12 (p+)
16 (n+)
15
11 (p+)
14
14
13
13
17 (p++)
9
11 (p+)
11 (p+)
10 (n)
12 (p+)
8 (p)
6 (n-)
4
1 (n)

Fig. 11



VERTICAL TRANSFER REGISTER
READ-OUT GATE
SENSOR
19
19
18
15
14
15
13
14
13
17 (p++)
9
16 (n+)
10 (n)
12 (p+)
11 (p+)
8 (p)
6 (n-)
4
1 (n)
10 (n)
12 (p+)
16 (n+)
17 (p++)
11 (p+)

Fig. 12



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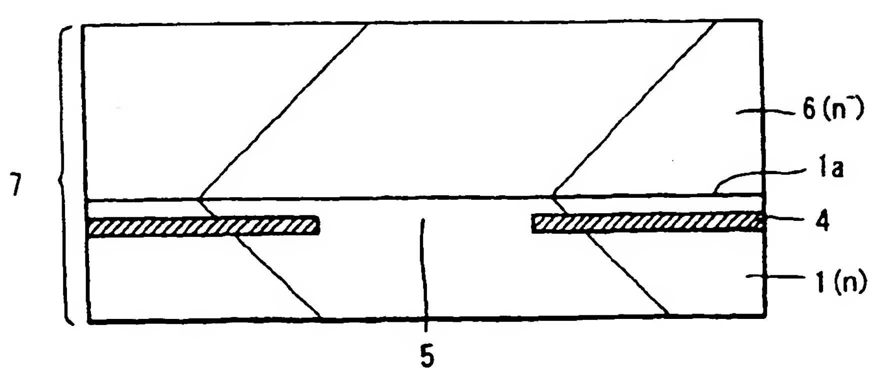
(54) **Epitaxial semiconductor substrate and manufacturing method thereof; manufacturing method of semiconductor device and of solid-state imaging device**

(57) Quality of epitaxial semiconductor substrates (7) treated by carbon gettering is evaluated precisely and quickly to use only good-quality ones for manufacturing good-property semiconductor devices, such as solid- state imaging devices. After carbon implanted regions (4) and carbon non-implanted regions (5) are made along the surface of a Si substrate (1) by selectively ion-implanting carbon, a Si epitaxial layer (6) is grown on the surface (1a) of the Si substrate (1) to obtain a Si epitaxial substrate (7). Recombination lifetime or surface photo voltage is measured at a portion of the Si epitaxial layer (6) located above the carbon non-implanted region (5), and the result is used to evaluate acceptability of the Si epitaxial substrate (7). Thus, strictly selected good-quality Si epitaxial substrates (7) alone are used to manufacture solid-state imaging devices or other semiconductor devices.

Fig. 5



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EUROPEAN SEARCH REPORT

Application Number
EP 99 40 0841

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 158 (E-1191), 17 April 1992 (1992-04-17) & JP 04 010544 A (HITACHI LTD), 14 January 1992 (1992-01-14) * abstract *	1,4,5	H01L31/18 H01L21/265 H01L21/74 H01L21/322
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A	JASTRZEBSKI L ET AL: "THE EFFECT OF HEAVY METAL CONTAMINATION ON DEFECTS IN CCD IMAGERS. \CONTAMINATION MONITORING BY SURFACE PHOTOVOLTAGE" JOURNAL OF THE ELECTROCHEMICAL SOCIETY,US,ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, vol. 137, no. 1, 1 January 1990 (1990-01-01), pages 242-249, XP000133076 ISSN: 0013-4651 * abstract * * page 248, column 1, paragraph 3; figure 19 *	9,12-14, 17,18	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 April 2000	Acco, S

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18-04-2000

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